modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of fabricating an array substrate, the method comprising:

forming a gate electrode on a substrate, a gate insulating layer on the gate electrode, an island-shaped oxide semiconductor layer on the gate insulating layer corresponding to the gate electrode;

forming an etch stopper on the oxide semiconductor layer and entirely over the substrate;

forming a source electrode, a drain electrode and a pixel electrode on the etch stopper, wherein the source and drain electrodes are spaced apart from each other with the oxide semiconductor layer therebetween, wherein the pixel electrode is connected to the drain electrode;

forming a first passivation layer on the source and drain electrodes and the pixel electrode and entirely over the substrate;

forming first and second separate regions including first and second contact holes, respectively, the first separate region is located where an end of the oxide semiconductor layer and an end of the source electrode opposing each other are formed, and the second separate region is located where the other end of the oxide semiconductor layer and an end of the drain electrode opposing each other are formed,

forming a conductive material layer at least in the first and second separate regions to form connection patterns which connect the oxide semiconductor layer to the source and drain electrodes at the first and second contact holes, respectively.

2. The method according to claim **1**, wherein forming of the first and second separate regions includes:

forming a first photoresist pattern on the first passivation layer corresponding to the gate electrode and including the first separate region where an end of the oxide semiconductor layer and an end of the source electrode opposing each other are formed, and the second separate region where the other end of the oxide semiconductor layer and an end of the drain electrode opposing each other are formed, wherein the first and second separate regions are formed by removing a first photoresist thereat;

removing the first passivation layer and the etch stopper at the first and second separate regions to form the first contact hole exposing the end of the oxide semiconductor layer and the end of the source electrode, and the second contact hole exposing the other end of the oxide semiconductor layer and the end of the drain electrode;

forming a conductive material layer on the first photoresist pattern and entirely over the substrate; and

selectively removing the conductive material layer to form connection patterns which connect the oxide semiconductor layer to the source and drain electrodes at the first and second contact holes, respectively.

3. The method according to claim **1**, wherein forming the gate electrode, the gate insulating layer, and the oxide semiconductor layer includes:

forming a first metal layer, a first insulating layer, an oxide semiconductor material layer sequentially on the substrate;

forming a second photoresist pattern and a third photoresist pattern on the oxide semiconductor material layer and having a first thickness and a second thickness, respectively, the second thickness is less than the first thickness;

etching the oxide semiconductor material layer, the first insulating layer and the first metal layer using the second and third photoresist patterns to form the gate electrode, the gate insulating layer and the oxide semiconductor patterns which have the same plane shape as that of the gate electrode;

performing an ashing to remove the third photoresist pattern;

removing the oxide semiconductor pattern exposed by removing the third photoresist pattern to form the island-shaped oxide semiconductor pattern which exposes both sides of the gate insulating layer; and

performing a stripping to remove the second photoresist pattern.

4. The method according to claim **1**, wherein forming the source electrode, the drain electrode and the pixel electrode on the etch stopper includes:

forming a transparent conductive material layer and a second metal layer on the etch stopper;

forming a fourth photoresist pattern and a fifth photoresist pattern on the second metal layer and having a third thickness and a fourth thickness, respectively, the fourth thickness is less than the third thickness;

etching the second metal layer and the transparent conductive material layer using the fourth and fifth photoresist patterns to form the source and drain electrodes, which each include a lower layer of transparent conductive material and an upper layer of second metal, and a pixel pattern which is in a pixel region and has the same structure as the drain electrode;

performing an ashing to remove the fifth photoresist pattern;

removing the upper layer of the pixel pattern exposed by removing the fifth photoresist pattern to form the pixel electrode made of transparent conductive material; and

performing a stripping to remove the fourth photoresist pattern.

5. The method according to claim **1**, further including:

forming a gate line on the substrate including a pixel region;

forming a gate pad electrode at an end of the gate line;

forming a data line on the etch stopper; and

forming a data pad electrode at an end of the data line, wherein the data line crosses the gate line to define the pixel region.

6. The method according to claim **1**, further including forming a second passivation layer on the first passivation layer and forming a gate pad contact hole exposing the gate pad electrode and a data pad contact hole exposing the data pad electrode, and forming a gate auxiliary pad electrode and forming a data auxiliary pad electrode on the second passivation layer which contacts the gate pad electrode and the data pad electrode through the gate pad contact hole and the data pad contact hole, respectively.

7. The method according to claim **2**, wherein selectively removing the conductive material layer to form the connection patterns includes:

forming an organic layer on the conductive material layer and filling the first and second separate regions;

performing an ashing to remove a portion of the organic layer on the conductive layer and form organic patterns which are other portions of the organic layer filling in the first and second separate regions and reduced in thickness by the ashing;